Low Power Square Root Carry Select Adder

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Abstract – Carry select adder is a fast adder, which uses multiple narrow adders and results fast wide adders. Carry select adders have great scope by reducing area, power consumption and delay. This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. Based on this modification 8, 16, 32, and 64-bit square-root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA architecture. Binary to Excess-1 Converter (BEC) is used instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption. The proposed CSLA design involves significantly less area and delay than the recently proposed BEC-based CSLA. In this paper the proposed design of 16bit regular SQRT CSLA is compared with modified version of SQRT CSLA. The result shows that modified SQRT CSLA is better than the regular CSLA.

Index Terms – Carry select adder (CSLA), Square Root CSLA (SQRT CSLA).

1. INTRODUCTION

Adders have a special significance in VLSI designs and it is used in computer and many other processors. It is used to calculate addresses, table indices and similar applications. Adders are also used in multipliers, in high speed integrated circuits and in digital signal processing. Nowadays design of low power and area efficient high speed data path logic systems are most substantial area in the research of VLSI design. Number of fast adders can be used for addition. In digital adders the sum of each bit position is added and the generated carry is propagated into the next position. The propagated carry reduces the speed of addition. The carry select adder can be used to alleviate this problem.

Carry select adder is one of the fastest adders having less area and power consumption. It generates partial sum and carry by considering carry input Cin=0 and Cin=1, the final sum and carry are selected by the multiplexers. The main idea used in this project is to use Binary to Excess-1 convertor (BEC) instead of RCA to reduce the area. This paper is organized in the following sections. II.Literature survey III.CSLA with BEC IV.Explanation about regular SQRT CSLA and modified SQRT CSLA V.Result VI.Synthesis report for regular 16-bit SQRT CSLA VII.Synthesis report for modified 16-bit SQRT CSLA VIII.Conclusion.

2. RELATED WORK

There are different types of fast adders used in processors such as ripple carry adder (RCA),carry look ahead adder (CLA)and carry select adder. Ripple carry adder provides compact design but their computation time is high. Carry look ahead adder gives fast result but it leads to an increase in area. Carry select adder provides a compromise between RCA and carry look ahead adder. Ripple carry adder produces worst case delay, because it consists of N single bit full adders. Each adder produces the sum and carry. The carry of the previous full adder is given as the input to the next adder. The carry is transferred through every stage and produces a delay called worst case delay. In ripple carry adder as value of N increases, delay also increases. So ripple carry adder has the lowest speed among the fast adders. The result is selected by the multiplexer.

The CSLA uses dual RCA's to generate partial sum and carry by considering Cin=0 and Cin=1 then the final sum and carry is selected by using multiplier. In regular CSLA area consumed is more due to the use of dual RCA's. The basic idea of this work is to use Binary to excess-1 convertor (BEC) instead of RCA with Cin=1to reduce the area and power. The advantage of BEC is that it uses less number of logic gates than N bit full adders. To reduce the delay N bit ripple carry adders are replaced with N+1 bit BEC .So modified SQRT CSLA is area consuming than regular CSLA.

3. CSLA with BEC

Modified CSLA uses BEC.BEC is a circuit used to add 1 to input numbers. The circuit of 4 bit BEC is shown in figure 2 and the truth table is shown in table 1.

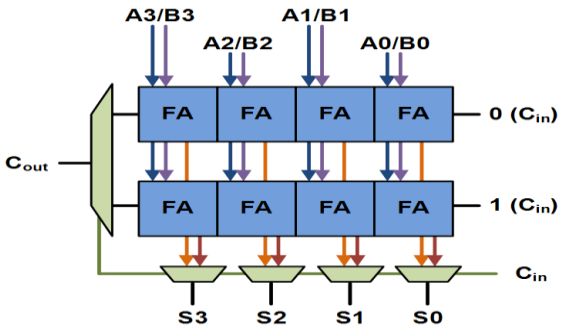

Fig1. Basic CSLA structure

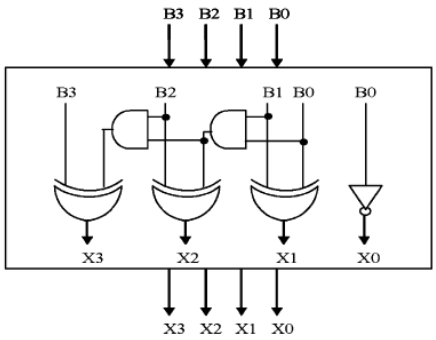

Fig2. 4-Bit Binary to Excess 1 Converter.

BEC consist of 4 inputs and the result is obtained by adding 1 with each of it. This logic is replaced in RCA with Cin=1. This logic can be implemented for different bits which are used in the modified design. The main advantage of this BEC logic comes from the fact that it uses lesser number of logic gates than the n-bit Full Adder (FA) structure. The BEC structure has a feature that it can perform the similar operation as that of the replaced RCA with Cin=1. The expressions of 4 bit BEC are listed below. The basic work is to use Binary to Excess-1 Converter (BEC) in the regular CSLA to achieve lower area and increased speed of operation. This logic is replaced in RCA with Cin=1. This logic can be implemented for different bits which are used in the modified design.

X0=~B0

X1=B0^B1

X2=B2^(B0&B1)

X3=B3^(B0&B1&B2)

Binary logic B0,B1,B2,B3	Excess-1logic X0,X1,X2,X3
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

Table1 Truth Table of 4 Bits Binary To Excess -1 Convertor

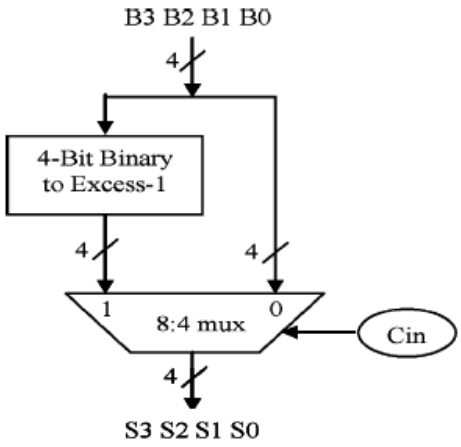

Fig3. 4 Bit Binary to excess-1 logic with 8:4 mux

Addition is achieved using BEC together with multiplexer as shown in figure 2 .If the select line of MUX is 0 then input is (B3,B2,B1 and B0) otherwise input is BECs output. Thus modified CSLA is designed such that it occupies less area and low power than regular CSLA. Also RCA is replaced with BEC.

4. DELAY AND AREA OF REGULAR 16 BIT ADDER

The delay can be calculated by adding up the number of gates in the longest path of logic block that contributes maximum delay. The area evolution is done by counting the total number of AOI gates required for each logic block. The structure of 16 bit regular SQRT CSLA is shown in fig 4, proposed design has five groups of different size RCA .Each group contain dual RCA and MUX. The delay and area of each group is calculated and at last finds the total area and delay. The main disadvantage of regular CSLA is high area usage that can be overcome by using modified CSLA.

Ripple-carry adders are the simplest and most compact full adders, but their performance is limited by a carry that must propagate from the least-significant bit to the most-significant bit. The various 16, 32, 64 and 128-bit CSLA can also be developed by using ripple carry adders. The speed of a carry-select adder can be improve, by performing the additions in parallel, and reducing the maximum carry delay.

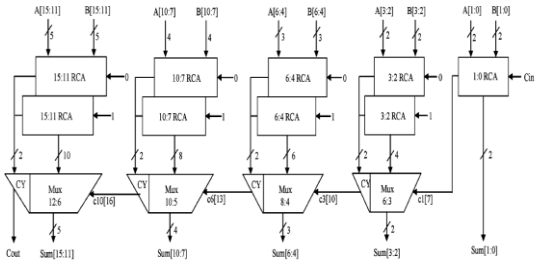

Fig4. Regular 16 bit SQRT CSLA

Modified SQRT CSLA is similar to that of regular SQRT CSLA the only difference we replace RCA with Cin=1 with BEC. The replaced BEC perform the same operation as that of the replaced RCA with C in=1.Figure 5 shows the modified SQTR CSLA. This structure consumes less area, delay and power than regular SQRT CSLA.

The modified block diagram is also divided into various groups of variable sizes of bits with each modified SQRT CSLA Group having the ripple carry adders, BEC and corresponding mux as shown in the Fig.5, Group 1 contain one RCA only which is having input of lower significant bit and carry in bit and produces result of sum and carry out which is acting as mux selection line for the next group, similarly the procedure continues for higher groups but they includes BEC logic instead of RCA with Cin=1.

Based on the consideration of delay values, the arrival time of selection input C1 of 8:3 mux is earlier than the sum of RCA and BEC. For remaining groups the selection input arrival is later than the RCA and BEC. Thus, the sum1 and c1 are depending on mux and results computed by RCA and BEC respectively. The sum2 depends on c1 and mux.

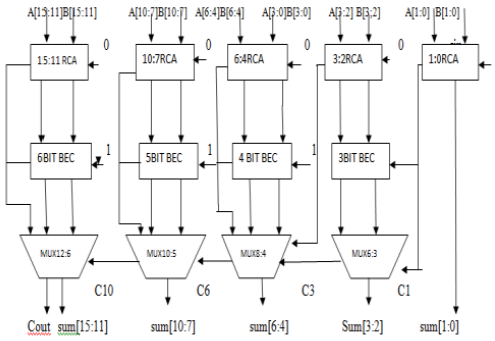

Fig 5. Modified 16-bit SQRT CSLA

5. RESULT

This work is developed using Xilinx tool. The area-efficient carry select adder achieves an outstanding performance in power consumption.

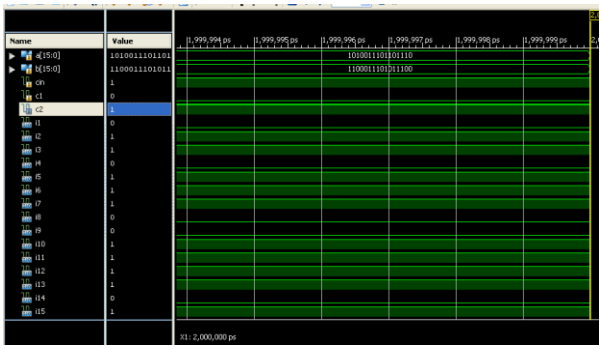

Fig 6. Output of Regular SQRT CSLA a (15:0) to i15

Power consumption can be greatly saved in our proposed area-efficient carry select adder because we only need XOR gate and as well as AND gate and OR gate in each carry-out operation. Modified SQRT CSLA has lesser number of logic gates and hence less area. The Xilinx ISE 9.2i software is used for synthesizing the adders, & Modelsim6.4a is used to compile & simulate to verify the VHDL code.

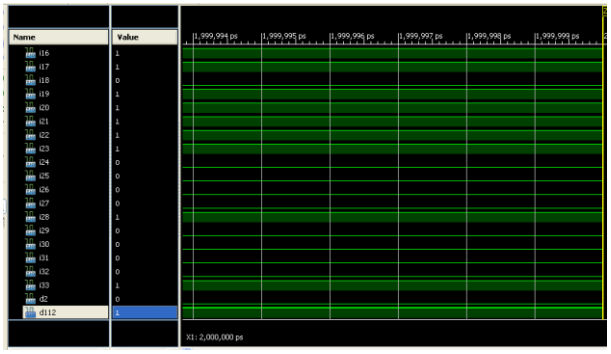

Fig7. Output of Regular SQRT CSLA i16 to d112

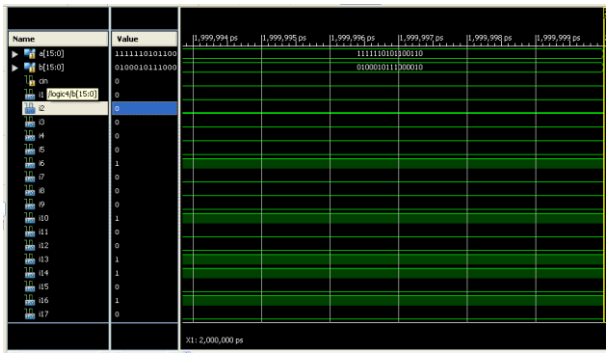

Fig 8.Output of Modified SQRT CSLA a (15:0) to i17

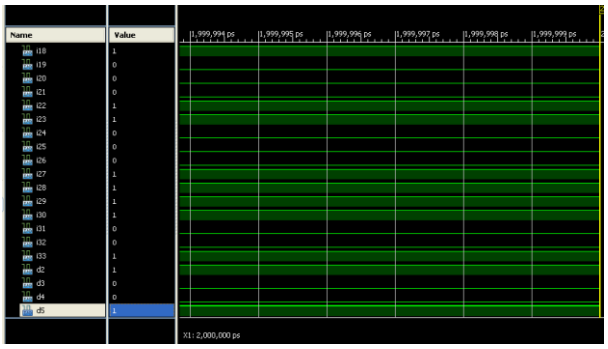

Fig 9. Output of Modified SQRT CSLA i18 to d5

6. SYNTHESIS REPORT FOR REGULAR 16-BIT SQRT CSLA

Total Delay: 12.172 ns

Total Memory usage is 140148 KB

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
No. of 4 Input LUT's	78	9.312	1%
No. of Occupied Slices	43	4.656	1%
Total no. of LUT's	78	9.312	1%
No. of Bonded IOB's	113	158	71%

7. SYNTHESIS REPORT FOR MODIFIED 16-BIT SQRT CSLA

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
No. of 4 Input LUT's	78	9.312	1%
No. of Occupied Slices	43	4.656	1%
Total no. of LUT's	78	9.312	1%
No. of Bonded IOB's	111	158	70%

Total Delay: 11.776 ns

Total Memory usage is 138100 KB

8. CONCLUSION

An efficient approach was proposed in this project to reduce the area of SQRT Carry Select Adder and a comparison of the advancements in the features of SQRT CSLA was discussed. The reduction in the number of gates was obtained by replacing the Ripple Carry Adder by Binary to Excess-1 Converter in the modified SQRT CSLA structure. The proposed design uses VHDL (Xilinx 12.1& 9.2i) module.

REFERENCES

[1] B. Ramkumar and Harish M Kittur, Low power and Area-Efficient Carry select adder, IEEE Trans. On VLSI Systems Vol. 20 Num.2 pp.371-375, February 2013.
[2] Alioto.M, Palumbo.G, "Analysis and comparison on full adder block in submicron technology, " IEEE Trans. On VLSI Systems, Vol. 10, pp. 806-823, Dec. 2011.
[3] Bedrij O. J., ―Carry-select adder,‖ IRE Trans. Electron. Comput., pp.340–344, 2012.
[4] Cadence, ―Encounter user guide,‖ Version 6.2.4, March 2008.
[5] Ceiang .T.Y , and Hsiao. M.J , ―Carry-select adder using single ripple carry adder,‖ Electron. Lett., vol. 34, no. 22, pp. 2101–2103.
[6] Chang Y. He, C. H.., and J. Gu, ―An area efficient 64-bit square root carry-select adder for low power applications,‖ in Proc. IEEE Int. Symp. Circuits Syst., 2005, vol. 4, pp. 4082–4085.
[7] Kim .Y and Kim. L.S, ―64-bit carry-select adder with reduced area ,‖ Electron Lett., vol. 37, no. 10, pp. 614–615, May 2010.
[8] Kuldeep Rawat, Tarek Darwish and magdy Bayoumi‖A low power and reduced area carry select adder‖.
[9] Cadence, ―Encounter user guide,‖ Version 6.2.4, March 2008.